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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/775,234	02/11/2004	Tae-Wook Kim	GK-US045033	9873

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EXAMINER	
LUU, AN T	

ART UNIT	PAPER NUMBER
2816	

DATE MAILED: 03/18/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/775,234	KIM ET AL.	
	Examiner	Art Unit	
	An T. Luu	2816	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *11 February 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-13* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-13* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *11 February 2004* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *2-11-04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Drawings

1. Figures 1 and 2 should be designated by a legend such as --Prior Art-- because only that which is old is illustrated. See MPEP § 608.02(g). Corrected drawings in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.84(c)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 112

2. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

3. Claim 7 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

As to claim 7, the limitation "a second voltage source, line 9, does not have a clear antecedent basis since there is no *a first voltage* source recited earlier.

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

5. Claims 6, 7 and 9 are rejected under 35 U.S.C. 102(b) as being anticipate by the Kimura reference (U.S. Patent 5,748,041).

Kimura discloses in figure 1 a mixing circuit comprising an amplification unit (i.e., Q3-5) having an input terminal (i.e., base of Q3) and an output terminal (i.e., emitter of Q3), and amplifying a signal Vc applied to the input terminal to output it to the output terminal; a mixing unit (Q1, Q2) having first, second and third input terminals (i.e., Vi+, Vi- and common node at emitter terminals), and first and second output terminals (i.e., Vout+ and Vout-), the third input terminal being connected to the output terminal of the amplification unit, the mixing unit mixing signals respectively applied to the first and second input terminals with a signal supplied to the third input terminal, to respectively output the mixed signals to the first and second output terminals (i.e., operational of an AGC amplifier circuit, see Abstract); and a current source 3 for providing a specific quantity of current to the third input terminal of the mixing unit as required by claim 6.

As to claim 7, the amplification unit (i.e., Q3-5) comprises an amplification element Q3 having a first terminal (base) that forms the input terminal, a second terminal (emitter) that forms the output terminal and a third terminal (collector), wherein the quantity and direction of current flowing from the second terminal to the third terminal are varied on the basis of the level of a voltage applied to the first terminal; and a degeneration impedance Q4 connected between the third terminal of the amplification element and a voltage source Vcc.

As to claim 9, figure 1 discloses the mixer circuit comprising a first amplification element Q1 having a first terminal (i.e., base) that forms the first input terminal, a second terminal (i.e., collector) that forms the first output terminal and a third terminal (i.e., emitter), wherein the quantity and direction of current flowing from the second terminal to the third terminal are varied on the basis of the level of a voltage applied to the first terminal; a second amplification element Q2 having a first terminal (base) that forms the second input terminal, a second terminal (collector) that forms the second output terminal, and a third terminal (emitter) connected to the third terminal of the first amplification element to form the third input terminal, wherein the quantity and direction of current flowing from the second terminal to the third terminal are varied on the basis of the level of the voltage applied to the first terminal (i.e., basis operation of a transistor); and first and second load impedances (R_L 7) connected between the second terminals of the first and second amplification elements and a voltage source Vcc, respectively.

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. Claims 1-4, 8 and 10-13 are rejected under 35 U.S.C. 103(a) as being obvious over the Kimura reference (U.S. Patent 5,748,041) in view of the Fong reference (U.S. Patent 6,147,559).

Kimura discloses a mixer circuit comprising all the claimed limitations as required by claim 8 except for teaching a capacitor connected between the first and second terminals of the amplification element as required by the claim.

Fong discloses in figure 1 an amplification element Q1 having a capacitor Cf coupled between the first and second terminals of the amplification element as required by claim 8.

It would have been obvious to one skilled in the art at the time the invention was made to incorporate the teaching of Fong into that of Kimura to reduce parasitic capacitance between terminals of a transistor.

A skilled artisan in the art would be motivated to utilize the teaching of Fong for the benefit of improving linearity and noise figure of the electronics circuit (i.e., mixer circuit).

As to claim 10, the scope of claim is similar to that of the combination of claims 6-8. Therefore, it is rejected for the same reasons set forth above.

As to claim 11, the scope of claim is similar to that of the combination of claims 6-9. Therefore, it is rejected for the same reason set forth above.

As to claim 12, it is noted that the teaching of Fong (i.e., the rejection of claim 8) is applicable to each amplification disclosed in Kimura.

As to claim 13, Kimura discloses in figure 1 a mixing circuit comprising an amplification unit (i.e., Q3-5) having an input terminal (i.e., base of Q3) and an output terminal (i.e., emitter of Q3), and amplifying a signal Vc applied to the input terminal to output it to the output terminal; a mixing unit (Q1, Q2) having first, second and third input terminals (i.e., Vi+, Vi- and common node at emitter terminals), and first and second output terminals (i.e., Vout+ and Vout-), the third input terminal being connected to the output terminal of the amplification unit, the mixing unit

mixing signals respectively applied to the first and second input terminals with a signal supplied to the third input terminal, to respectively output the mixed signals to the first and second output terminals (i.e., operational of an AGC amplifier circuit, see Abstract) wherein the mixing circuit includes a first amplification element Q1 having a first terminal (base) that forms the first input terminal, a second terminal (collector) that forms the first output terminal and a third terminal (emitter), the quantity and direction of current flowing from the second terminal to the third terminal being varied on the basis of the level of a voltage applied to the first terminal; a second amplification element Q2 having a first terminal that forms the second input terminal, a second terminal (collector) that forms the second output terminal, and a third terminal (emitter) connected to the third terminal of the first amplification element to form the third input terminal, the quantity and direction of current flowing from the second terminal to the third terminal being varied on the basis of the level of the voltage applied to the first terminal; and first and second load impedances (R_L 7) connected between the second terminals of the first and second amplification elements and a voltage source Vcc, respectively as partially required by claim 13.

Kimura does not disclose first and second capacitors, the first capacitor being connected between the first and second terminals of the first amplification element, the second capacitor being connected between the first and second terminals of the second amplification element as required by the claim.

Fong discloses in figure 2 an amplification element Q1 having a capacitor Cf coupled between the first and second terminals of the amplification element as required by claim 8.

It would have been obvious to one skilled in the art at the time the invention was made to incorporate the teaching of Fong into that of Kimura to reduce parasitic capacitance between terminals of a transistor.

A skilled artisan in the art would be motivated to utilize the teaching of Fong for the benefit of improving linearity and noise figure of the electronics circuit (i.e., mixer circuit).

As to claim 1, Kimura discloses in figure 1 a mixing circuit comprising an amplification unit (i.e., Q3-5) having an input terminal (i.e., base of Q3) and an output terminal (i.e., emitter of Q3), and amplifying a signal Vc applied to the input terminal to output it to the output terminal; a mixing unit (Q1, Q2) having first, second and third input terminals (i.e., Vi+, Vi- and common node at emitter terminals), and first and second output terminals (i.e., Vout+ and Vout-), the third input terminal being connected to the output terminal of the amplification unit, the mixing unit mixing signals respectively applied to the first and second input terminals with a signal supplied to the third input terminal, to respectively output the mixed signals to the first and second output terminals (i.e., operational of an AGC amplifier circuit, see Abstract); and a current source 3 for providing a specific quantity of current to the third input terminal of the mixing unit as partially required by the claim.

Kimura does not disclose a capacitor connected between the amplification unit and the mixing unit as required by the claim.

Fong discloses in figure 2 an amplification unit comprising a capacitor C1 for coupling between the amplification unit and the mixer circuit (col. 1, line7-11).

It would have been obvious to one skilled in the art at the time the invention was made to incorporate the teaching of Fong into that of Kimura to reduce noise of the amplification unit.

A skilled artisan in the art would be motivated to utilize the teaching of Fong for the benefit of improving linearity and noise figure of the electronics circuit (i.e., mixer circuit).

As to claim 2, Fong discloses in figure 2 an amplification element Q1 having a first terminal (base) that forms the input terminal, a second terminal (collector) that forms the output terminal and a third terminal (emitter), wherein the quantity and direction of current flowing from the second terminal to the third terminal are varied on the basis of the level of a voltage applied to the first terminal (as shown); a load impedance R1 connected between the second terminal of the amplification element and a first voltage source Vcc; and a degeneration impedance Ze connected between the third terminal of the amplification element and a second voltage source (ground).

As to claim 3, the scope of claim is similar to that of claim 8. Therefore, it is rejected for the same reason set forth above.

As to claim 4, figure 1 discloses the mixer circuit comprising a first amplification element Q1 having a first terminal (i.e., base) that forms the first input terminal, a second terminal (i.e., collector) that forms the first output terminal and a third terminal (i.e., emitter), wherein the quantity and direction of current flowing from the second terminal to the third terminal are varied on the basis of the level of a voltage applied to the first terminal; a second amplification element Q2 having a first terminal (base) that forms the second input terminal, a second terminal (collector) that forms the second output terminal, and a third terminal (emitter) connected to the third terminal of the first amplification element to form the third input terminal, wherein the quantity and direction of current flowing from the second terminal to the third terminal are varied on the basis of the level of the voltage applied to the first terminal (i.e., basis

operation of a transistor); and first and second load impedances (R_L 7) connected between the second terminals of the first and second amplification elements and a voltage source Vcc, respectively.

8. Claim 5 is rejected under 35 U.S.C. 103(a) as being unpatentable over the Kimura reference (U.S. Patent 5,748,041) in view of the Fong reference (U.S. Patent 6,147,559 and further in view of the Abou-Allam et al reference (U.S. Patent 6,094,084).

The combination of Kimura and Fong discloses all the claimed invention of claim 5 except for having a current constructed by an LC circuit as particular required by the claim.

Abou-Allam discloses in figure 2 a mixing circuit including a current source being constructed by an LC circuit as required by the claim.

It would have been obvious to one skilled in the art at the time the invention was made to incorporate the teaching of Abou-Allam into that of Kimura and Fong since a current source is known to be implemented in many different ways. One of them is taught by the Abou-Allam reference.

A skilled artisan would be motivated to utilize the LC current source taught by Abou-Allam would provide a circuit having a narrowband characteristic and there is no voltage drop across LC circuit which is suitable in an environment required a small power source (i.e., low voltage battery).

Conclusion

9. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to An T. Luu whose telephone number is 571-272-1746. The examiner can normally be reached on 7:30-5:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Timothy P. Callahan can be reached on 571-272-1740. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

An T. Luu
3-14-05

Terry D. Cunningham
Primary Examiner